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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,442	03/01/2006	Mun-Pyo Hong	PNK-0242	7000

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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
06/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,442	HONG ET AL.	
	Examiner	Art Unit	
	RON E. POMPEY	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *5-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner's Note: the only changes to the mailing, 1/9/08, is correction to the PTOL-326 to have only box 2b checked.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6091466), in view of Kim (US 6624871).

Kim('466) discloses the limitations of:

Claim 1. A thin film transistor array panel comprising:

an insulating substrate (101, fig. 5A)

a gate wire formed on the substrate and including a gate line (113/113a, fig. 5B) and a gate electrode (111, fig. 5B) connected to the gate line (fig. 4);

a gate insulating layer (117, fig. 5C) formed on the gate line; a semiconductor layer (133, fig. 5C) formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a data line (123, fig. 5D) intersecting the gate line (fig. 4), a source electrode (121, fig. 5D) connected to the data line, and a drain electrode (131, fig. 5D) located opposite the source electrode with respect to the gate electrode;

a pixel electrode (141, fig. 5F) connected to the drain electrode; and

an etching assistant pattern (133a, fig. 5C) made of the same layer as the semiconductor pattern (133, fig. 5C) and located out of an area defined by intersections of the gate line and the data line (fig. 4), wherein the etching assistant pattern is extended from the semiconductor layer (col.5, ln. 15 – col. 6, ln. 37).

Claim 2. The thin film transistor array panel of claim 1, wherein the data wire (123/121/131, fig. 5D) comprises a lower film of Cr, Mo or Mo ally (col. 5, ln. 53-60).

Claim 3. The thin film transistor array panel of claim 2, further comprising a passivation layer (137, fig. 5D) disposed between the data wire and the pixel electrode.

Claim 4. The thin film transistor array panel of claim 3, wherein the semiconductor layer has substantially the same planar shape as the data wire except for a channel portion located between the data line and the drain electrode.

13. The thin film transistor array panel of claim 1, wherein the etching assistant pattern is located outside of a pixel area (133, fig. 4).

14. The thin film transistor array panel of claim 1, wherein the etching assistant pattern is formed directly on the gate insulating layer (133, fig. 5C).

3. Kim (‘466), as indicated above, discloses all the features of the claims except:

Claim 2. The thin film transistor array panel of claim 1, wherein the data wire comprises an upper film of Al or Al ally.

a. However, Kim(‘871) discloses:

The thin film transistor array panel of claim 1, wherein the data wire comprises a lower film of Cr, Mo or Mo ally and an upper film of Al or Al ally (35S/35D/35P/35L, fig. 4A; col. 4 , lns. 28-31 Kim).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the data wire in Kim ('466), with the dual layer with a lower film of Cr, Mo or Mo ally and an upper film of Al or Al ally as taught by Kim('871), because the Al provides for excellent electrical conductivity of the data wire.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4 and 13-14, received 10-30-07, have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RON E. POMPEY whose telephone number is (571)272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

Ron Pompey
AU: 2812
1/4/08